REMARKS

The Final Office Action mailed on April 6, 2001, has been received and reviewed. Claims 31-45 are currently pending in the application. Claims 31-45 stand rejected. It is proposed that claim 36 be canceled without prejudice or disclaimer. Reconsideration of the application is respectfully requested.

Claim Objections

Claims 33, 34, and 45 were provisionally objected to under 37 C.F.R. § 1.75 as being substantial duplicates of claims 31, 32, and 44.

It is respectfully submitted that, in view of the proposed amendments to claims 33, 34, and 45 presented herein, claims 33, 34, and 45 are no longer substantial duplicates of claims 31, 32, and 44.

Accordingly, it is respectfully requested that the objections to claims 33, 34, and 45 under 37 C.F.R. § 1.75 be withdrawn.

Rejections Under 35 U.S.C. § 102

Park

Claims 31-34 and 38-41 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,457,063 to Park (hereinafter "Park").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Park discloses a high surface area storage cell for a capacitor and a method for fabricating the same. The storage cell of Park is formed from polysilicon and includes downwardly extending recesses. These downwardly extending recesses are formed by forming an insulating layer over the polysilicon from which the storage cell is to be formed, forming polysilicon *pieces* on the insulating layer, using the polysilicon pieces as a mask during etching of the insulating layer, and using the remaining portions of the insulating layer as a mask for patterning the

polysilicon of the storage cell. Col. 1, line 47, to col. 2, line 9. As depicted in FIG. 1A of Park, the polysilicon pieces 10 are spaced apart from one another. As recesses are being formed in the polysilicon of the storage cell, the polysilicon pieces are removed from the insulating layer. Col. 2, lines 7-9.

Independent claim 31, as presented and proposed to be amended herein, recites a semiconductor capacitor storage poly that comprises "downwardly extending recesses" and "a plurality of contiguous mesas forming a maze-like structure."

While Park discloses a storage poly that includes downwardly extending recesses, Park does not disclose that the portions of the storage poly that remain adjacent to the recesses comprise "a plurality of contiguous mesas forming a maze-like structure." Rather, Park discloses that pieces of polysilicon are used as a mask for patterning another mask from an underlying insulating layer. These pieces of polysilicon are depicted in FIG. 1A of Park as being separate and spaced apart from one another. When the insulating layer mask is being formed, the polysilicon pieces prevent removal of underlying regions of the insulating layer. Thus, the portions of the storage poly that remain following patterning thereof through the insulating layer mask are at substantially the same locations as were the separate, spaced apart polysilicon pieces. Thus, as illustrated in FIGs. 2 and 4 of Park, the portions of the storage poly that remain following patterning of the storage poly are small, individual protrusions, rather than contiguous mesas.

Therefore, it is respectfully submitted that Park does not anticipate each and every element of independent claim 31, as proposed to be amended. Accordingly, independent claim 31, as proposed to be amended, is allowable under 35 U.S.C. § 102(b).

Claim 32 is allowable, among other reasons, as depending from claim 31, which should be allowed.

Independent claim 33, as presented and proposed to be amended herein, recites a semiconductor capacitor storage poly that comprises "downwardly extending recesses", "a plurality of contiguous webs forming a maze-like structure", and "hemispherical-grain polysilicon on top surfaces of at least some of said plurality of contiguous webs."

By way of contrast, Park lacks disclosure of both "contiguous webs" and "hemispherical-grain polysilicon on top surfaces of at least some . . . contiguous webs". Rather, as indicated

with reference to the rejection of independent claim 31, Park shows and discloses a storage poly that includes small, individual protrusions rather than contiguous webs. Further, Park discloses, at col. 2, lines 7-9, that "[u]pon etching the . . .[storage poly], the polysilicon pieces 10 . . . are removed."

It is, therefore, respectfully submitted that Park does not disclose each and every element of independent claim 33, as proposed to be amended, and that independent claim 33 is allowable under 35 U.S.C. § 102(b).

Claim 34 is allowable, among other reasons, as depending from claim 33, which is allowable.

Chang

Claims 37, 44, and 45 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,723,373 to Chang et al. (hereinafter "Chang").

Chang also discloses a semiconductor device capacitor. Among other things, Chang discloses an intermediate storage node structure that includes a polysilicon member 10 with hemispherical-grain polysilicon 12 on a surface thereof, microgrooves 14 formed in the polysilicon member, referred to as a conductive member 10, and located laterally between elevated regions of the hemispherical-grain polysilicon 12, and a silicon oxide layer 16 filling the microgrooves 14 and covering the hemispherical-grain polysilicon 12 (FIG. 4; col. 4, lines 33-50).

Independent claim 37, as presented and proposed to be amended herein, recites an intermediate semiconductor memory cell structure that comprises, among other things, "recesses formed in [a] storage poly structure and located laterally between . . . low elevation regions of [a] hemispherical-grain polysilicon layer" on the storage poly structure.

As Chang discloses and illustrates microgrooves 14 that are located between elevated regions of a hemispherical-grain polysilicon layer, rather than "between . . . low elevation regions of [a] hemispherical-grain polysilicon layer", as is recited in independent claim 37, it is respectfully submitted that Chang does not disclose each and every element of independent claim 37, as proposed to be amended.

Accordingly, it is respectfully submitted that independent claim 37, as proposed to be amended, is allowable under 35 U.S.C. § 102(e).

Independent claim 44, as presented and proposed to be amended herein, recites an intermediate semiconductor capacitor structure that includes, among other things, "a mask overlying at least portions of [a] hemispherical-grain polysilicon layer . . ."

Chang does not disclose that a mask overlies portions of the hemispherical-grain polysilicon layer of any of the intermediate semiconductor capacitor structures illustrated and disclosed therein. Rather, at col. 4, lines 33-37, Chang discloses that the hemispherical-grain polysilicon layer 12 is used "as a mask to form a rugged surface of the first conductive layer 10", or microgrooves 14 in the conductive layer 10.

Accordingly, it is respectfully submitted that Chang does not disclose each and every element of independent claim 44, as proposed to be amended. It is, therefore, respectfully submitted that independent claim 44, as proposed to be amended, is allowable under 35 U.S.C. § 102(e).

Independent claim 45, as presented and proposed to be amended herein, recites an intermediate semiconductor memory cell that includes, among other things, a storage poly structure, a hemispherical-grain polysilicon layer on at least portions of the storage poly structure, "a mask overlying at least . . . low elevation regions of [the] hemispherical-grain polysilicon layer", and recesses that are formed in the storage poly structure and "exposed between [the] low elevation regions of [the] hemispherical-grain polysilicon layer and through [the] mask . . ."

By way of contrast with independent claim 45, as proposed to be amended, Chang lacks disclosure of a mask, as well as recesses that are exposed both between low elevation regions of a hemispherical-grain polysilicon layer and through a mask. Rather, Chang teaches, at col. 4, lines 33-37, that the hemispherical-grain polysilicon layer 12 itself serves as a mask for patterning the conductive layer 10 and consequently that the microgrooves 14 are located laterally between elevated regions of the hemispherical-grain polysilicon layer 12.

It is, therefore, respectfully submitted that Chang does not disclose each and every element of independent claim 45, as proposed to be amended. Accordingly, it is respectfully submitted that independent claim 45, as proposed to be amended, is allowable under 35 U.S.C. § 102(e).

Wu

Claim 42 stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,814,549 to Wu (hereinafter "Wu").

A precursor to, or intermediate of, the semiconductor device capacitor disclosed in Wu and depicted in FIG. 7 thereof includes, among other things, a polysilicon storage node 26 and silicon islands 28 that have been formed from hemispherical-grain polysilicon on a surface of the polysilicon storage node 26. At col. 4, lines 26-27, Wu teaches that the hemispherical-grain polysilicon is slightly etched to form separate silicon islands 28. A spin-on-glass (SOG) etch mask 30 is formed on the surface of the polysilicon storage node 26 and laterally between the silicon islands 28, with elevated portions of the silicon islands 28 protruding through the etch mask 30.

Independent claim 42, as presented and proposed to be amended herein, recites an intermediate semiconductor capacitor structure that includes, among other things, "a substantially confluent hemispherical-grain polysilicon layer on [a] storage poly structure . . ." Independent claim 42 also recites that "elevated portions of [the] hemispherical-grain polysilicon layer [are] exposed through [the] mask."

While Wu discloses that elevated portions of the silicon islands 28 protrude through the etch mask 30 thereof, Wu clearly does not disclose the hemispherical-grain polysilicon layer from which the separate silicon islands 28 are formed is confluent.

Accordingly, it is respectfully submitted that Wu does not disclose each and every element of independent claim 42, as proposed to be amended. It is, therefore, submitted that independent claim 42 is allowable under 35 U.S.C. § 102(e).

For these reasons, it is respectfully requested that the Office withdraw the 35 U.S.C. § 102 rejections of claims 31-34, 37-42, 44, and 45.

Rejections Under 35 U.S.C. § 103(a)

Ahn in View of Wu

Claims 35, 36, and 43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,358,888 to Ahn et al. (hereinafter "Ahn") in view of Wu.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Ahn teaches methods for fabricating capacitor structures for use in semiconductor devices. An intermediate structure formed in the method of Ahn includes a conductive layer 40b, a first material layer 50b overlying conductive layer 40b, and islands of hemispherical-grain polysilicon, which are collectively referred to as HSG layer 80, on first material layer 50b (FIG. 13; col. 8, lines 22-28. A subsequent intermediate structure, which is illustrated in FIG. 14 of Ahn, includes recesses that are formed in conductive layer 40b, separating sections 40c thereof, and located laterally between elevated regions of the HSG layer 80 (*see,* col. 8, lines 32-35, which indicates that HSG layer 80 is used as an etch mask to pattern first material layer 50b and that the patterned first material layer 50c is, in turn, used as a mask for the patterning of conductive layer 40b).

The teachings of Wu have been summarized previously herein.

It is respectfully submitted that the asserted combination of Ahn and Wu does not render any of claims 35, 36, or 43 obvious under 35 U.S.C. § 103(a) for several reasons.

One of Ordinary Skill in the Art Would Not Have Been Motivated to Make the Proposed Combination

First, it is respectfully submitted that one of ordinary skill in the art would not have been motivated by Ahn, Wu, or the knowledge that was generally available in the art prior to the

priority date for the referenced application to combine the teachings of Ahn and Wu in the manner that has been suggested in the outstanding Final Office Action.

Specifically, Ahn discloses a process that includes etching between silicon islands and, thus, between elevated regions of hemispherical-grain polysilicon to form a mask from an underlying layer that is subsequently used to pattern underlying conductive material of a storage node. Consequently, recesses in the storage node are formed laterally between the elevated regions of the hemispherical-grain polysilicon, while the portions of the storage node that remain are located beneath the elevated regions of the hemispherical-grain polysilicon. In contrast, the method disclosed in Wu includes forming spaced apart silicon islands from hemispherical-grain polysilicon, forming a spin-on-glass mask layer laterally between the silicon islands, and etching the silicon islands and regions of a storage node structure that underlie the silicon islands through the mask. The result of the method disclosed in Wu is an intermediate storage node structure with recesses that are located beneath the previous positions of the silicon islands.

As the structures of Ahn and Wu include recesses that are formed in opposite locations, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of these references in the manner that has been asserted. Rather, it appears, based upon the very different teachings of Ahn and Wu, that any motivation to combine the teachings of these references could only have been gleaned from the disclosure of the referenced patent application.

The References Teach Away from The Proposed Combination

Second, it is respectfully submitted that, when considered together, Ahn and Wu both teach away from the proposed combination.

In pertinent part, M.P.E.P. § 2141.02 provides:

> A prior art reference must be considered in its entirety, i.e., as a whole, *including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc., v. Garlock, Inc.,* 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied,* 469 U.S. 851 (1984). (Italicized emphasis supplied).

Because the recesses of the storage poly structures disclosed in Ahn and Wu are formed by methods that cause the recesses to be located in opposite positions (*i.e.,* laterally between the locations of silicon islands in Ahn and beneath the positions of silicon islands in Wu), it is

respectfully submitted that each of these references teaches away from combining the teachings thereof with the other of these references.

There Is No Reasonable Expectation that the Proposed Combination Would Be Successful

Third, it is respectfully submitted that there is no reasonable expectation that the proposed combination of Ahn and Wu would successfully provide the structures recited in any of claims 35, 36, or 43.

When the teachings of Ahn and Wu are considered in their entireties, as required by M.P.E.P. § 2141.02, the resulting structure would include recesses positioned beneath the previous locations of the elevated regions of the silicon islands and laterally between the previously locations of the elevated regions of the silicon islands. Thus, if the teachings of Ahn and Wu were combined, no storage node material would remain.

It is, therefore, respectfully submitted that no reasonable expectation exists that, by combining the teachings of Ahn and Wu, a storage poly including the features of any claims 35, 36, or 43 could be produced.

The Proposed Combination Does Not Teach or Suggest Each and Every Claim Element

Fourth, it is respectfully submitted that Ahn and Wu, taken either alone or in combination, do not teach or suggest each and every element of any of claims 35, 36, or 43.

Independent claim 35, as presented and proposed to be amended herein, recites an intermediate semiconductor capacitor structure that includes, among other things, a storage poly structure, recesses formed in the storage poly structure, "a hemispherical-grain polysilicon layer over [the] storage poly structure", and that the recesses are exposed through the hemispherical-grain polysilicon and a mask.

Neither Ahn nor Wu teaches or suggests an intermediate structure that includes a storage poly structure with recesses formed therein and a hemispherical-grain polysilicon layer on the storage poly structure. Rather, at col. 8, lines 37-39, teaches that the hemispherical-grain polysilicon layer of the intermediate structure thereof "is eliminated together with the conductive layer [40b]" as recesses are formed in the conductive layer 40b. Wu similarly teaches, at col. 2,

lines 37-38, and at col. 4, lines 45-47, that the hemispherical-grain polysilicon "is totally removed" as recesses are being formed in the storage node.

Claim 36 is allowable, among other reasons, as depending from claim 35, which is allowable.

Independent claim 43, as presented and proposed to be amended herein, recites an intermediate semiconductor capacitor structure that includes, among other things, "a mask positioned over [a] hemispherical-grain polysilicon layer and spaced apart from [a] storage poly structure by [the] hemispherical-grain polysilicon structure.

In contrast to independent claim 43, as proposed to be amended, neither Ahn nor Wu teaches or suggests a structure that includes a mask positioned over hemispherical-grain polysilicon and spaced apart from a storage poly by way of the hemispherical-grain polysilicon. Rather, Ahn teaches a structure that includes a mask located between hemispherical-grain polysilicon and a storage node, while Wu teaches a structure that includes a mask located on a surface of a storage node, between silicon islands formed from hemispherical-grain polysilicon.

In view of the foregoing, it is respectfully submitted that each of claims 35, 36, and 43 is allowable under 35 U.S.C. § 103(a). Withdrawal of the 35 U.S.C. § 103(a) rejections of each of these claims is, therefore, respectfully requested.

ENTRY OF AMENDMENTS

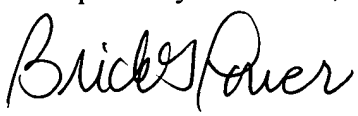
The proposed amendments to claims should be entered because the proposed amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. In addition, it is respectfully submitted that the proposed amendments do not raise new issues or require a further search. The proposed amendments also represent a good faith effort to place the claims in condition for allowance. In addition, the amendments proposed herein could not have been presented previously, as they are at least in part responsive to new grounds of rejection first raised in the outstanding Office Action. Further, for the purpose of appeal, it is respectfully submitted that the proposed amendments narrow the issues remaining in the case. Finally, if it is determined that the proposed amendments do not place the

application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 31-35 and 37-45 are believed to be in condition for allowance. An early indication of the allowability of each of these claims is respectfully solicited, as is an notice that the case has been passed for issuance. If any issues preventing the allowance of any of claims 31-35 and 37-45 remains that might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully Submitted,



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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

31. (Twice amended) A semiconductor capacitor storage poly, comprising: [including]downwardly extending recesses[formed therein, said recesses comprising]; and a plurality of contiguous mesas forming a maze-like structure.

33. (Twice amended) A semiconductor capacitor storage poly, comprising: [including]downwardly extending recesses[formed therein, said recesses comprising]; a plurality of contiguous webs forming a maze-like structure; and hemispherical-grain polysilicon on top surfaces of at least some of said plurality of contiguous webs.

35. (Amended) An intermediate semiconductor capacitor structure, comprising: a storage poly structure with recesses formed therein; a hemispherical-grain polysilicon layer over said storage poly structure; and a mask over said hemispherical-grain polysilicon layer, [portions of] said recesses being exposed through said hemispherical-grain polysilicon layer [being exposed through] and said mask.

37. (Amended) An intermediate semiconductor memory cell structure, comprising: a storage poly structure[with recesses formed therein]; low elevation regions of a hemispherical-grain polysilicon layer on said storage poly structure; recesses formed in said storage poly structure and located laterally between said low elevation regions of said hemispherical-grain polysilicon layer; and dielectric material at least lining the recesses.

38. (Amended) A semiconductor memory cell structure, comprising:

a storage poly structure;

regions of hemispherical-grain polysilicon on at least portions of an upper surface of said storage poly structure;

a plurality of recesses extending into said storage poly structure, at least some recesses of said plurality of recesses being located laterally between said regions of hemispherical-grain polysilicon; and

and a dielectric layer substantially coating an upper surface of said storage poly structure and substantially lining each of said plurality of recesses.

42. (Amended) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure;

a substantially confluent hemispherical-grain polysilicon layer on said storage poly structure; and

a mask positioned over [the] said substantially confluent hemispherical-grain polysilicon layer, elevated portions of [the] said hemispherical-grain polysilicon layer being exposed through said mask.

43. (Amended) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure including recesses formed therein;

a hemispherical-grain polysilicon layer on at least portions of said storage poly structure; and

a mask positioned over [the] said hemispherical-grain polysilicon layer and spaced apart from said storage poly structure by said hemispherical-grain polysilicon layer, said recesses in said storage poly structure being exposed through said mask.

44. (Amended) [A] An intermediate semiconductor capacitor structure, comprising:

a storage poly structure with recesses formed therein;

a hemispherical-grain polysilicon layer on at least portions of the storage poly structure;

a mask overlying at least portions of said hemispherical-grain polysilicon layer; and

dielectric material lining at least said recesses.

45. (Amended) [A] An intermediate semiconductor memory cell structure, comprising:

a storage poly structure with recesses formed therein;

low elevation regions of a hemispherical-grain polysilicon layer on at least portions of the storage poly structure;

a mask overlying at least said low elevation regions of said hemispherical-grain polysilicon layer, said recesses being exposed between said low elevation regions of said hemispherical-grain polysilicon layer and through said mask; and

dielectric material at least lining said recesses.